IN THE SPECIFICATION:

1. Please replace page 1 with the following text:

MULTI-STANDARD TURBO INTERLEAVER USING TABLES

PRIORITY

This application claims priority to an application entitled "Interleaver for a turbo encoder and decoder" filed at the UK Patent Office on December 11, 2003 and assigned Serial No. GB0328783.6.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an interleaver for a turbo encoder and decoder.

2. Description of the Related Art

Wireless communication systems are widely deployed to provide various types of communications such as voice and data. One such system is wide band code division multiple access WCDMA, which has been adopted in various competing wireless communication standards, for example 3rd generation partnership project 3GPP and 3GPP2.

To overcome data corruption that can occur during RF transmission the different wireless communication standards typically include some form of channel coding, where one common channel coding technique is turbo coding.

Turbo coding involves the use of a turbo encoder for encoding a code segment (i.e. a data packet) and a turbo decoder for the decoding of the encoded code segment.

As shown in figure 1, a turbo encoder 100 includes two convolutional encoders 101, 102 and an interleaver 103, where the interleaver 103 shuffles (i.e. interleaves) the information bits in the packet in accordance with a specified interleaving scheme.

2. Please replace page 2 with the following text:

The turbo encoder 100 uses a first convolutional encoder 101 to encode information bits (i.e. systematic bits) within a code block to generate a first sequence of parity bits (i.e. parity 1 bits) in parallel to the interleaver 103 shuffling the information bits, where the shuffled information bits are encoded by a second encoder 102 to generate a second sequence of parity bits (i.e. parity 2 bits). The information bits and the parity bits in the first and second sequence are then modulated and transmitted to a receiver.

The information bits and the first and second sequence of parity bits are received by a receiver and decoded by a turbo decoder.

With reference to figure 2, the turbo decoder 200 initially stores the received information bits and the parity bits in the first and second sequence in a buffer (not shown). Initially, the information bits and the first sequence of parity bits from the first convolutional encoder are retrieved from the buffer and decoded by a first decoder 201 (i.e. a first soft in soft out SISO decoder) to provide 'extrinsic' information (i.e. a-posteriori data) indicative of adjustments in the confidence in the detected values for the information bits. In one embodiment, intermediate results (i.e. a-priori) that include the extrinsic information from the first decoder 201 are then stored in the buffer in an interleaved order matching the code interleaving used at the transmitter. Alternatively, embodiment the extrinsic information from the first decoder (i.e. first SISO decoder) can be stored in the buffer in a non-interleaved order and read from the buffer in an interleaved order.

The intermediate results, the information and the second sequence of parity bits from the second encoder are retrieved from the buffer and decoded by a second decoder 202 (i.e. a second SISO decoder) to provide extrinsic information indicative of further adjustments in the confidence in the detected values for the information bits. Intermediate results that comprise the extrinsic information from the second decoder 202 (i.e. a second SISO decoder) are then stored in the buffer in a deinterleaved order complementary to the code interleaving performed at the transmitter. Alternatively, the extrinsic information can be stored in an interleaved order and read from the buffer in a deinterleaved order. The intermediate results are used in a next decoding iteration performed by the turbo decoder 200. The

3. Please replace page 3 with the following text:

turbo decoder 200 performs a predetermined number of decoding iterations before producing a decision on the value of the decoded information bit.

Accordingly, the interleaving and deinterleaving of data is an important aspect of turbo encoding and decoding.

However, the interleaving and deinterleaving specifications that form part of the turbo coding/decoding process can be different for the different wireless communication standards. As such, dual standard wireless communication devices, for example a 3GPP and 3GPP2 compliant radiotelephone, typically require multiple interleavers and deinterleavers to accommodate the different standards, which can result in increased die size, power consumption and cost.

It is desirable to improve this situation.

SUMMARY OF THE INVENTION

In accordance with a first aspect of the present invention there is provided an interleaver for a turbo encoder or decoder according to claim 1.

This provides the advantage of allowing a single interleaver to support more than one wireless communication standard.

In accordance with a second aspect of the present invention there is provided a method for interleaving for a turbo encoder and decoder.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the invention will now be described, by way of example, with reference to the drawings, of which:

Figure 1 illustrates a known turbo encoder;

Figure 2 illustrates a known turbo decoder;

4. Please replace page 4 with the following text:

Figure 3 illustrates a turbo decoder according to an embodiment of the present invention;

Figure 4 illustrates an address generation unit according to an embodiment of the present invention;

Figure 5 illustrates a feature of an address generation unit according to an embodiment of the present invention;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 3 shows a turbo decoder 300. The turbo decoder 300 includes a first SISO decoder 301, a second SISO decoder 302, a first memory module 303 and a second memory module 304.

The first SISO decoder 301 has a first maximum a posterior MAP decoding module 305 for executing a MAP algorithm, a first address generation unit AGU 306 and a first buffer 307.

The first MAP decoding module 305 is arranged to receive information bits and parity 1 bits from a transmitting unit (not shown) with the first AGU 306 producing linear address sequences to allow the first MAP decoding module 305 to read intermediate results (i.e. a priori data) from the second memory module 304 and write extrinsic information (i.e. a-posterior data) generated by the first MAP decoding module 305 to the first memory module 303.

The second SISO decoder 302 has a second maximum a posterior MAP decoding module 308 for executing the MAP algorithm, a second address generation unit AGU 309 and a second buffer 310.